REMARKS

Applicant amended claims 12 and 13 to correct typographical errors. Claims 1-4, 6-8, 10-14 and 17-26 are pending in the above-identified application. Claims 1, 17, and 22 are independent.

The examiner rejected claims 1-4, 5, 6-9, 11-14 and 17-23 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,928,358 to Takayama, in view of U.S. Patent No. 5,724,563 to Hasegawa. The examiner also rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Takayama in view of Hasegawa, and further in view of U.S. Patent No. 5,274,770 to Khim Yeoh et al. The examiner further rejected claims 24-26 under 35 U.S.C. §103(a) as being unpatentable over Takayama in view of Hasegawa, and further in view of U.S. Patent No. 5,923,872 to Chrysos.

Specifically, the examiner stated:

> 3. As to the newly amended claim 1, the newly amended feature of the bit and the register being specified in the branch instruction does not affect the original scope of the bit specified in the branch instruction of a register specified in the branch instruction. Takayama did teach the bit [20b] being specified in the branch instruction (see fig.3 branch instruction format). (Final Action, Page 2)

Additionally, responding to the arguments presented in applicant's Amendment in Reply to Office Action of May 8, 2006, the examiner further stated:

> 9. As to b), Takayama is also directed to executing a branch instruction [20] that identifies a particular bit location [1 bit] of a particular register [20b] whose content (1,0) will determine if branching operation is performed (see col.7, lines 38-51).
>
> 10. As to c), applicant only recites "...a bit of a register being set or clear, the bit and the register being specified in the branch instruction...". Takayama's prediction bit [20b] was specified in the branch instruction [20] (see fig.3). (Final Action, Page 4)

Applicant respectfully disagrees with the examiner's contentions

Applicant's independent claim 1 recites "executing a branch instruction in execution of an instruction stream with a branch based on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction." Thus, applicant's branch instruction identifies a particular register, and a particular bit of that register, whose content (i.e. "1" or "0") will determine if the branching operation is performed.

In contrast, Takayama describes an apparatus to facilitate branching prediction functionality. With respect to the branch instruction illustrated in FIG. 3, Takayama explains that:

> **FIG. 3 shows the branch instruction format of the information processing apparatus 100. A branch instruction 20 is composed of a 13-bit operation code 20a, 1-bit branch prediction information 20b, 2-bit branch history information 20c and a 16-bit branch destination address 20d. The operation code 20a shows an operation code and a branch condition which identify the present instruction.**
>
> **The branch prediction information 20b predicts whether the branch is taken or not taken when the present branch instruction is next executed. The relation between the branch prediction information 20b and the prediction is as follows: when the branch prediction information 20b is "0", a branch is predicted "not taken"; and when the branch prediction information 20b is "1", a branch is predicted "taken". (Col. 7, lines 38-44)**

Thus, Takayama's branch instruction does not specify a particular bit of a particular register. Rather, Takayama's branch instruction includes a branch prediction bit that specifies whether branching is to be taken or not. For example, if the branch prediction bit indicates that branching is to be taken (i.e., Takayama's branch instruction is predicting that the branch condition that is yet to be determined will result in a decision to branch), then the next instruction from the instruction stream that Takayama's apparatus fetches is the instruction at the branched-out address. But that branch prediction bit does not identify a register, and/or a bit of that register, whose content will determine if branching is to be performed. Accordingly, Takayama neither discloses nor suggests at least the feature of "executing a branch instruction in execution of an instruction stream with a branch based on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction," as required by applicant's independent claim 1.

Further responding to the applicant's arguments presented in the Amendment in Reply to Action of May 8, 2006, the examiner stated:

> 13. As to f), applicant never claimed that the branch operation itself, which is to be performed by the executing stage, is based on the value of a particular bit of a particular register specified by the instruction that was decoded. Instead, applicant claimed "executing a branch instruction" and " before performing the branch operation ". No execution stage of the branch operation itself can be found, applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlaq. 113, USPQ 530, 534 (1957)).

As noted above, applicant's independent claim 1 recites "with a branch ***based*** on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction" (emphasis added). Thus, contrary to the examiner's contention, applicant's claim 1 does recite that the branching operation is based on a value of a particular bit of a particular register.

As for Hasegawa, as explained in applicant's Amendment in Reply to Office Action of May 8, 2006, Hasegawa also does not disclose or suggest at least the feature of "executing a branch instruction in execution of an instruction stream with a branch based on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction," as required by applicant's independent claim 1. Indeed, the examiner admitted in the Final Action that Hasegawa is being relied upon for the purpose of:

> 12. As to e), Hasegawa was used to supplement the teaching of specifying number of instructions in the instruction stream (see fig.10, number 3 specified in the branch instruction). The reasons of obviousness were already given in the last Office action in on paragraph 4 on 05/08/06. Therefore, it will not be repeated herein. (Final Action, Page 4)

Because neither Takayama nor Hasegawa discloses or suggests, alone or in combination, at least the feature of "executing a branch instruction in execution of an instruction stream with a branch based on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction," applicant's independent claim 1 is patentable over the cited art.

Claims 2-4, 6-8, 14 and 24 depend from independent claim 1 and are therefore patentable for at least the same reasons as independent claim 1.

Independent claim 22 recites "execute a branch instruction in execution of an instruction stream in the processor, with a branch operation based on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction." For reasons similar to those provided with respect to applicant's independent claim 1, at least this feature is not disclosed by the cited art. Accordingly, applicant's independent claim 22 is patentable over the cited art.

Claims 23 and 26 depend from applicant's independent claim 22 and are therefore patentable for at least the same reasons as independent claim 22.

With respect to applicant's independent claim 17, the examiner stated in the May 8, 2006, Office Action:

> 14. As to claim 17, Takayama taught executing a branch instruction that causes a branch operation in an instruction stream based on any specified value being true or false (see the execution unit judgi [*sic*] the condition of the branch instrcuin [*sic*] in col.13, ines 29-39). (Office Action, Page 5)

Applicant's respectfully disagrees with the examiner's contention.

With respect to the execution stage of its hardware, Takayama describes:

> **During the first half of the clock cycle 3 (3a), the instruction executing unit 15 judges the condition of the branch instruction in accordance with the control signal from the instruction decoding unit 14. After this, the instruction executing unit 15 informs the branch history information generating unit 16 and the branch prediction information generating unit 17 of the execution result (whether the branch was taken or not taken), as well as informing the instruction decoding unit 14 and the address control unit 8 of the prediction result (whether the prediction was correct or incorrect). (Col. 13, lines 29-39)**

Takayama further explains that:

> **The instruction decoding unit 14 is achieved by a ROM storing a microprogram or the like, and decodes the operation code 13a of an instruction stored in the instruction register 13 before outputting the decoding result as a control signal 141 to the instruction executing unit 15. When a branch instruction is subject to the decoding process, the instruction decoding unit 14 informs the instruction executing unit 15 and the address control unit 8 of the branch prediction information 13b of the branch instruction via a signal line 142. (Col. 8, lines 39-48)**

Accordingly, one control signal provided by decoding unit 14 indicates what operation, corresponding to the decoded instruction, is to be performed. When the decoded instruction is a branch instruction, the decoding unit 14 also provides the branch prediction signal that indicates the branch prediction of the branch instruction, and thus indicates whether branching is to be taken before Takayama's apparatus determines the branch condition. But at no point does Takayama disclose that the branch operation itself is based on the value of a particular bit of a particular register specified by the instruction that was decoded by decoding unit 14.

For the foregoing reasons, and for reasons similar to those provided with respect to independent claim 1, the prior art does not disclose or suggest at least the feature of "executing a branch instruction that causes a branch operation in an instruction stream based on a bit of a register being set or cleared, the bit and the register being specified in the branch instruction," as

required by applicant's independent claim 17. Applicant's independent claim 17 is thus patentable over the prior art.

Claims 18-21 and 25 depend from independent claim 17 and are therefore patentable for at least the same reasons as independent claim 17.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

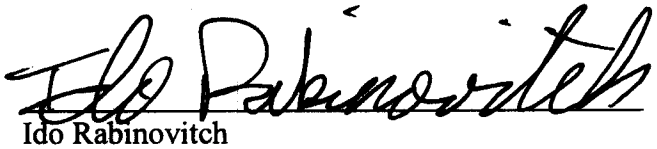
Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges to deposit account 06-1050, referencing the attorney docket shown above.

Respectfully submitted,

Date: Nov. 14, 2006



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